CLAIMS

1. A process for fabricating high-voltage drain-extension transistors, whereby the transistors are integrated in a semiconductor substrate along with non-volatile memory cells that include floating gate transistors, said process comprising at least the following steps:

defining respective active areas for HV transistors and floating gate transistors in a common semiconductor substrate, with said active areas being separated from each other by insulating regions;

depositing a layer of gate oxide onto said active areas;

depositing a layer of polysilicon onto the gate oxide layer;

first masking and then etching through the polysilicon layer to form gate regions of said HV transistors;

performing a first dopant implantation to form first junction portions of the HV transistors;

conformably depositing a dielectric layer onto the whole substrate to provide an interpoly layer of said floating gate transistor;

forming openings at the first junction portions of the HV transistors; and

performing, through said openings, a second dopant implantation to form second junction portions of the HV transistors, with perimeter areas of the gate regions and the active areas of the floating gate transistors being screened off by said dielectric layer.

2. A process according to claim 1, wherein said second junction portions of the HV transistors are shallower than said first junction portions of the HV transistors.

3. A process according to claim 1, further comprising a step of siliciding said second junction portions of the HV transistors.

4. A high-voltage transistor integrated in a semiconductor substrate with a first type of conductivity, comprising a gate region comprised between corresponding drain and source junctions, wherein said junctions comprise first regions lightly doped with a second type of conductivity and heavily doped second regions with the second type of conductivity, wherein said more doped second regions lie centrally within said lightly doped first regions such that first and second portions of the first regions are positioned immediately adjacent to opposite sides of the second regions.

5. The transistor of claim 4, further comprising a thin dielectric layer that covers said drain and source junctions only at locations of said first and second portions of said lightly doped first regions

6. The transistor of claim 5 wherein the thin dielectric layer extends on and completely across the gate region and on the first portions of the drain and source junctions, which are adjacent to the gate region.

7. A memory device integrated in a semiconductor substrate, comprising:

a floating gate memory transistor having a gate positioned on the substrate and source and drain regions positioned in the substrate at opposite sides of a channel region positioned under the gate, the gate including a gate dielectric layer positioned on the channel region, a conductive floating gate region positioned on the gate dielectric layer, and an intermediate dielectric layer positioned on the floating gate region; and

a high voltage transistor having a gate positioned on the substrate and source and drain regions positioned in the substrate at opposite sides of a channel region positioned under the gate of the high voltage transistor, wherein at least one of the source and drain regions includes a lightly doped first region that is overlaid by the

intermediate dielectric layer and a highly doped second region positioned within the first region and below an opening in the intermediate dielectric layer.

8. The memory device of claim 7, wherein the second region is centrally located within the first region such that first and second portions of the first region are positioned immediately adjacent to opposite sides of the second region.

9. The transistor of claim 7 wherein the intermediate dielectric layer extends on and completely across the gate of the high voltage transistor and on the first portion of the first region, which is immediately adjacent to the channel region of the high voltage transistor.

10. A method of fabricating a memory device integrated in a semiconductor substrate, the memory device including a high voltage transistor, the method comprising:

forming a gate that includes a gate dielectric on the substrate and a conductive gate layer on the gate dielectric;

performing a first dopant implantation to form first junction regions on opposite sides of a channel region underlying the gate;

forming a dielectric layer on the gate and on the first junction regions;

forming an opening in the dielectric layer above a central portion of one of the first junction portions, the opening being defined by first and second portions of the dielectric layer that are on opposite sides of the opening and above the one of the first junction portions; and

performing, through the opening, a second dopant implantation to form a second junction portion within the central portion, while the first and second portions of the dielectric area screen off peripheral portions of the one of the first junction portions.

11. The method claim 10, wherein the second junction portion is shallower than the first junction portions of the high voltage transistor.

12. The method claim 10, further comprising siliciding the second junction portion of the high voltage transistor.

13. The method of claim 10 wherein:

forming the gate includes forming a gate dielectric of a floating gate transistor integrated in the substrate and forming from the conductive gate layer a floating gate on the gate dielectric of the floating gate transistor;

performing the first dopant implantation includes forming junction regions on opposite sides of a channel region underlying the gate dielectric of the floating gate transistor;

the dielectric layer is formed on the floating gate to form an intermediate dielectric layer of the floating gate transistor; and

the method further includes forming a control gate on the intermediate dielectric layer.

14. The method of claim 10 wherein forming the gate includes forming an insulated gate of a low voltage transistor, the dielectric layer is formed on the insulated gate and on portions of the substrate at which source and drain regions of the low voltage transistor will be formed, forming the opening includes removing the dielectric layer from the portions of the substrate at which the source and drain regions of the low voltage transistor will be formed, and performing the second dopant implantation includes forming the source and drain regions of the low voltage transistor.

15. A process for fabricating high-voltage drain-extension transistors, whereby the transistors are integrated in a semiconductor substrate along with non-

volatile memory cells that include floating gate transistors, the process comprising at least the following steps:

defining respective active areas for HV transistors and floating gate transistors in a common semiconductor substrate, with the active areas being separated from each other by insulating regions;

forming insulated gate regions of the HV transistors;

performing a first dopant implantation to form first junction portions of the HV transistors;

conformably depositing a dielectric layer onto the whole substrate to provide an interpoly layer of the floating gate transistor;

forming openings at the first junction portions of the HV transistors; and

performing, through the openings, a second dopant implantation to form second junction portions of the HV transistors, with perimeter areas of the gate regions and the active areas of the floating gate transistors being screened off by the dielectric layer.

16. A process according to claim 15, wherein the second junction portions of the HV transistors are shallower than the first junction portions of the HV transistors.

17. A process according to claim 15, further comprising a step of siliciding the second junction portions of the HV transistors.

18. A process according to claim 15 wherein the openings in the dielectric layer are above respective central portions of the first junction portions, each of the openings being defined by respective first and second portions of the dielectric layer that are on opposite sides of the opening and above the first junction portions; wherein the second junction portions are within the central portion and are completely surrounded by the first junction portions.

19. A process according to claim 15 wherein forming the insulated gate regions includes forming an insulated gate of a low voltage transistor, the dielectric layer is formed on the insulated gate and on portions of the substrate at which source and drain regions of the low voltage transistor will be formed, forming the openings includes removing the dielectric layer from the portions of the substrate at which the source and drain regions of the low voltage transistor will be formed, and performing the second dopant implantation includes forming the source and drain regions of the low voltage transistor.